National Aeronautics and Space Administration

Electrical and Electronics

N Channel JFET Based Digital Logic Gate Structure

A breakthrough in SiC semiconductors allowing for operating temperatures up to 600°C

Innovators at NASA's Glenn Research Center have developed and patented a digital logic device that enables simplified silicon carbide (SiC) sensors and electronics to operate at remarkably high temperatures (up to 600°C) with greater endurance and more sophistication than ever before. This technology utilizes unique circuit topography to create usable digital logic gates with N (negatively doped) channel junction field effect transistors (JFETs), load resistors, level shifting resistors, and supply rails. This novel device, which was originally developed for planetary exploration, allows for digital logic at temperatures that exceed what is currently considered to be state-of-the-art for SiC devices (300°C to 500°C). Consequently, it can operate reliably and efficiently in extremely harsh environments, such as inside automotive engines or within nuclear reactors. Its compact design allows for enhanced multiplexer constructs such as memory and decoding, giving it a clear advantage over preexisting SiC technologies.

BENEFITS

- Robust: Enables the use of simplified SiC-based electronics and digital logic in high-temperature and radiation environments
- Efficient: Features a source-coupled topography that allows for resources to be used elsewhere to add more integrated circuit features
- Space-saving: Allows for the construction of AND/OR (sum of products) arrays which use far fewer transistors and resistors than arrays constructed from existing gates
- Power-saving: Works with fewer level shifters, reducing power dissipation
- Versatile: Allows for configuration into a driver for oscillator circuits, allowing for time bases and simple digitizers for resistive/reactive sensors

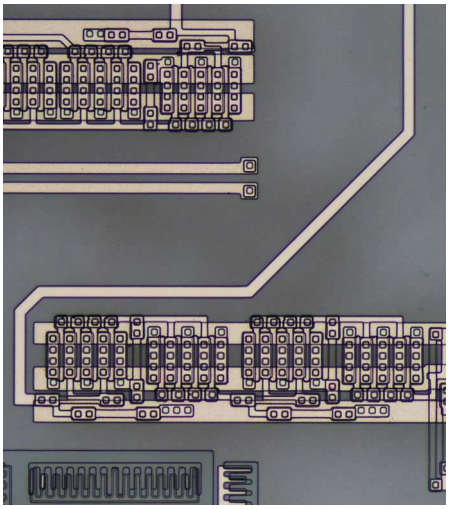
technology solution

THE TECHNOLOGY

In 2010, NASA Glenn Research Center secured a patent for an innovative approach to SiC component production (described in U.S. Patent 7,688,117) that enabled the development of logic gates using only epitaxial resistors and N channel JFETs. This allowed for the production of pulse and edge triggered latches through the use of inverting and combinatorial logic. This innovation was improved upon in 2013 and a second patent was issued. In the modified version of this technology, epitaxial resistors are used as loads and level shifters to create useable logic blocks with N channel JFETs. The resistive level shifter can be designed at the output of the basic gate structure, or at the input, which means that the device can be considered a lone follower transistor with its source node as the output of the gate. The basic logic gate can be configured as a driver for oscillator circuits, allowing for time bases and simple digitizers for resistive or reactive sensors.

By removing the level shifter from the output of the gate structure, this new adaptation boasts a simplified source-coupled gate topography, which makes more real estate available for other circuit functions. Furthermore, by replacing multiple paths to the ground (level shifter strings) with a single path to the ground, power is saved and the device operates more efficiently.

NASA's unique digital logic device enables machines such as this Mars Rover to perform more efficiently in extremely harsh environments.



This technology features a unique adaptation with a Multi-Level Interconnect Integrated Circuit.

APPLICATIONS

The technology has several potential applications:

- Oil & gas drilling
- Aviation
- Automotive
- High-temperature wireless sensors
- Nuclear reactors
- Robotics
- Geothermal sensing
- Planetary exploration
- Hydrothermal vents

PUBLICATIONS

Patent No: 7,688,117; 8,416,007

More Information

National Aeronautics and Space Administration

Technology Transfer Office

Glenn Research Center

21000 Brookpark Road
Cleveland, OH 44135
216-433-3483
ttp@grc.nasa.gov

http://technology.nasa.gov/

www.nasa.gov

NP-2015-04-1511-HQ

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LEW-18256-1, LEW-18636-1